

CLAIMS

What is claimed is:

- 1 1. A method comprising:
2 fixing a logical identifier for a signal line at an egress interface;
3 mapping a first physical identifier for a first physical signal line to the
4 logical identifier; and
5 remapping a second physical identifier for a second physical signal line
6 to the logical identifier responsive to a line failure on the first physical signal line.
- 1 2. The method of claim 1 wherein mapping comprises:
2 writing to a cross connect table and wherein remapping comprises
3 rewriting the cross connect table.
- 1 3. The method of claim 1 further comprising:
2 switching a signal from a second physical signal line to a physical line
3 corresponding to the logical identifier responsive to the remapping.
- 1 4. The method of claim 1 wherein fixing comprises:
2 assigning an identifier to each port of the egress interface during
3 initialization; and
4 preventing change to the identifier after initialization.
- 1 5. The method of claim 1 wherein the signal line is a synchronous optical
2 networking (SONET) line.
- 1 6. An apparatus comprising:
2 a bus interface;
3 an ingress time slot interchange (ITSI) module;
4 a switch fabric coupled to the ITS module;
5 an egress time slot interchange (ETSI) module having a plurality of
6 inputs, each input assigned a logical identifier which remains fixed after
7 initialization; and

8 a translation module to translate an incoming signal identifier to one
9 of the logical identifiers independent of a physical line on which the signal is
10 received.

1 7. The apparatus of claim 6 wherein the translation module comprises:
2 a cross connect table.

1 8. The apparatus of claim 1 further comprising:
2 a bus coupled to the bus interface;
3 a termination module coupled to the bus; and
4 a line interface having an optical to electrical (O/E) and electrical to
5 optical (E/O) converter.

9. The apparatus of claim 6 wherein the apparatus is implemented as an
ASIC on a backplane of a line card.

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